



Devineni Venkata Ramana & Dr. Hima Sekhar

# MIC College of Technology

(AUTONOMOUS)

Date: 26-04-2023

## External Lab (Supple) Schedule April 2023

### B.Tech V Sem Supple. – MIC18

| Branch | Date       | Name of the Lab                        | 9:30-12:30 | 1.00-4.00 |
|--------|------------|----------------------------------------|------------|-----------|
| ECE    | 08-05-2023 | Digital Signal Processing Lab-18EC5L09 | ALL        | -         |

### B.Tech V Sem Supple. – MIC20

| Branch | Date       | Name of the Lab                                        | 9:30-12:30 | 1.00-4.00 |
|--------|------------|--------------------------------------------------------|------------|-----------|
| CIVIL  | 08-05-2023 | Geotechnical Engineering LAB-20CE5L07                  | ALL        | -         |
|        | 08-05-2023 | Skill Oriented Course -3 (STAAD PRO)-20CE5L09          | ALL        | -         |
| EEE    | 08-05-2023 | Control Systems LAB-20EE5L10                           | ALL        | -         |
|        | 09-05-2023 | Electrical Simulation LAB-20EE5L11                     | -          | ALL       |
|        | 09-05-2023 | JAVA Programming-20EE5S12                              | ALL        | -         |
|        | 08-05-2023 | Summer Internship-20EE5I14                             | -          | ALL       |
| MECH   | 09-05-2023 | Simulation of Mechanical Systems Lab -20ME5S11         | ALL        | -         |
| ECE    | 08-05-2023 | Digital System Design using VHDL& Verilog LAB-20EC5L11 | ALL        | -         |
|        | 09-05-2023 | Micro Processors and Micro Controllers LAB-20EC5L10    | ALL        | -         |

## Mandatory Course (Supple) Schedule April 2023

| Branch | Date       | Name of the Lab                                  | 9:30-12:30 |
|--------|------------|--------------------------------------------------|------------|
| EEE    | 09-05-2023 | Essence of Indian Traditional knowledge-20EE5M13 | ALL        |



Chief Superintendent

CHIEF SUPERINTENDENT  
DVR & Dr. HS MIC College of Technology  
Kanchikacherla, NTR Dt,  
Andhra Pradesh, India - 521180.



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## V Sem Supple MIC18 Supple. Labs –Apr-2023

|            |     |   |          |                               |
|------------|-----|---|----------|-------------------------------|
| 18H71A04G3 | ECE | 5 | 18EC5L09 | Digital Signal Processing Lab |
|------------|-----|---|----------|-------------------------------|

## V Sem Supple MIC20 Supple. Labs –Apr-2023

| REGNO      | GRP   | SEM | PCODE    | PNAME                                            |
|------------|-------|-----|----------|--------------------------------------------------|
| 20H71A0117 | CIVIL | 5   | 20CE5L10 | Geotechnical Engineering Lab                     |
| 21H75A0137 | CIVIL | 5   | 20CE5L10 | Geotechnical Engineering Lab                     |
| 20H71A0108 | CIVIL | 5   | 20CE5S12 | STAAD PRO LAB                                    |
| 20H71A0119 | CIVIL | 5   | 20CE5S12 | STAAD PRO LAB                                    |
| 20H71A0450 | ECE   | 5   | 20EC5L10 | Microprocessors and Microcontrollers Lab         |
| 20H71A0466 | ECE   | 5   | 20EC5L10 | Microprocessors and Microcontrollers Lab         |
| 20H71A0469 | ECE   | 5   | 20EC5L10 | Microprocessors and Microcontrollers Lab         |
| 20H71A04C6 | ECE   | 5   | 20EC5L10 | Microprocessors and Microcontrollers Lab         |
| 20H71A04E2 | ECE   | 5   | 20EC5L10 | Microprocessors and Microcontrollers Lab         |
| 20H71A04E3 | ECE   | 5   | 20EC5L10 | Microprocessors and Microcontrollers Lab         |
| 21H75A0410 | ECE   | 5   | 20EC5L10 | Microprocessors and Microcontrollers Lab         |
| 20H71A0414 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 20H71A0494 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 20H71A04A7 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 20H71A04B4 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 20H71A04B8 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 20H71A04C6 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 20H71A04D9 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 20H71A04E2 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 20H71A04E4 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 21H75A0403 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 21H75A0405 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 21H75A0413 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 21H75A0440 | ECE   | 5   | 20EC5L11 | Digital system Design using VHDL and Verilog Lab |
| 20H71A0201 | EEE   | 5   | 20EE5I14 | Summer Internship                                |
| 20H71A0225 | EEE   | 5   | 20EE5I14 | Summer Internship                                |
| 20H71A0225 | EEE   | 5   | 20EE5L10 | Control Systems Lab                              |
| 20H71A0225 | EEE   | 5   | 20EE5L11 | Electrical Simulation Lab                        |
| 21H75A0253 | EEE   | 5   | 20EE5M13 | Essence of Indian Traditional knowledge          |
| 20H71A0225 | EEE   | 5   | 20EE5S12 | JAVA Programming                                 |
| 21H75A0307 | MECH  | 5   | 20ME5S11 | Simulation of Mechanical Systems Lab             |



  
PRINCIPAL

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